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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,082	10/30/2003	Armin Willmeroth	MUH-12838	9900

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,082	WILLMEROTH ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5-12 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/03; 2/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I in the reply filed on November 1, 2004 is acknowledged.

Applicant indicated that claims 1-4, 6, and 13-19 read on the elected species. However, a quick review of the drawings indicates that claim 6, which claims the emitter short regions are integrated in insular fashion, does not read on the elected species. Therefore, claims 5, 6, 7-12, and 20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claim Objections

Claim 16 is objected to because of the following informalities: there is insufficient antecedent basis for "the one hand". It is suggested the limitations "on the one hand" and "on the other hand" be removed from the claim, since use of these expressions does not help to further define the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki (US Pat. 6,323,509).

Regarding claim 1, Figure 1 of Kusunoki discloses an IGBT with a monolithically integrated antiparallel diode, comprising: a semiconductor substrate 1 forming an inner zone and having a front side, a rear side, and a peripheral high-voltage edge (region where p-regions 28 are located); said front side of said semiconductor substrate having semiconductor wells 8 of a first conductivity type (p-type) formed therein with transistor cells within said peripheral high-voltage edge; at least emitter region 4 of the first conductivity type formed at said rear side of said semiconductor substrate; at least one emitter short region 6 of a second conductivity type integrated substantially only in a region of said high voltage edge, said at least one emitter short region lying in a plane with said at least one emitter region and forming an electrode of the antiparallel diode; said at least one emitter region having no emitter short regions within said high-voltage edge; and said semiconductor wells on said front side of said semiconductor substrate forming a counterelectrode of the antiparallel diode. Note that it is considered that the gate electrodes 11 dissect region 8 into a plurality of separate wells.

Regarding claim 2, Figure 1 of Kusunoki discloses said semiconductor wells 8 at least predominately contain transistor cells.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (US Pat. 4,689,647, hereinafter Nakagawa).

Regarding claim 1, Figure 6 of Nakagawa discloses an IGBT with a monolithically integrated antiparallel diode, comprising: a semiconductor substrate 12 forming an inner zone

and having a front side, a rear side, and a peripheral high-voltage edge (region to the right of region 14-4); said front side of said semiconductor substrate having semiconductor wells (13-1 and 13-2) of a first conductivity type (p-type) formed therein with transistor cells within said peripheral high-voltage edge; at least emitter region 11 of the first conductivity type formed at said rear side of said semiconductor substrate; at least one emitter short region 21 of a second conductivity type integrated substantially only in a region of said high voltage edge, said at least one emitter short region lying in a plane with said at least one emitter region and forming an electrode of the antiparallel diode; said at least one emitter region having no emitter short regions within said high-voltage edge; and said semiconductor wells on said front side of said semiconductor substrate forming a counterelectrode of the antiparallel diode.

Regarding claim 2, Figure 6 of Nakagawa discloses said semiconductor wells (13-1 and 13-2) at least predominately contain transistor cells.

Regarding claim 3, Figure 6 of Nakagawa discloses said at least one emitter short region 21 reaches as far as a chip end in edge portions of the IGBT.

Regarding claim 4, Figure 6 of Nakagawa discloses edge regions of the IGBT contain an emitter region 11 at said high-voltage edge.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Pat. 4,893,165, hereinafter Miller) in view of the Hajime et al. ("Effects of Shorted Collector..., hereinafter Hajime).

Regarding claims 13 and 19, Figure 1 of Miller discloses an IGBT with a monolithically integrated antiparallel diode, comprising: a semiconductor substrate 1 forming an inner zone and having a front side, a rear side, and a peripheral high-voltage edge; said front side of said semiconductor substrate having semiconductor wells 5 of a first conductivity type (p-type) formed therein with transistor cells within said peripheral high-voltage edge; at least emitter region 15 of the first conductivity type formed at said rear side of said semiconductor substrate; said emitter region having a thickness of less than 1 micrometer and a doping with a does of between $1x10^{12}$ and $1x10^{15}$ charge carriers per cm^2 (col. 2, lines 64-68). The difference between Miller and the claimed invention is having emitter short region. Figure 1a of Hajime discloses emitter short regions in a plane with emitter regions and forming an electrode of an antiparallel diode. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Miller by using an emitter short region for the purpose of reducing the turn off time (see Introduction section of Hajime).

Regarding claim 14, Miller discloses a lifetime of minority charge carriers is at least 10 microseconds (col. 3, lines 20-23).

Regarding claim 15, Miller discloses a thickness of said inner zone formed by said substrate is less than 200 microns (col. 3, lines 15-18).

Regarding claim 17, Miller discloses said substrate 2 forming said inner zone is weakly doped, and said emitter region 15 is heavily doped with a significantly higher doping concentration than said inner zone (col. 2, lines 58-60).

Regarding claim 18, Miller discloses said at least one emitter region is annealed at a temperature of less than 600 degrees C (col. 3, lines 36-39).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller as applied to claim 13 above, and further in view of Nakagawa.

A further difference between Miller and the claimed invention is a field stop region of the second conductivity type (n-type) integrated between said substrate and said emitter region and emitter short region. Figure 6 of Nakagawa discloses a field stop region (buffer region) between the substrate 12 and the emitter and emitter short regions (11 and 21, respectively). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Miller by including a field stop region for the purpose of decreasing the on-resistance (col. 4, lines 55-58 of Nakagawa).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

January 6, 2005